

WHAT IS CLAIMED IS:

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1. A CMOS sensor circuit comprising:  
a photodiode;  
a reset transistor resetting said  
photodiode to an initial voltage; and  
10 a voltage control circuit controlling a  
gate potential of said reset transistor to a  
potential other than power source potentials.

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2. A CMOS sensor circuit comprising:  
a photodiode;  
a reset transistor resetting said  
20 photodiode to an initial voltage; and  
a voltage control circuit keeping a gate  
potential of said reset transistor from completely  
becoming off.

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3. The CMOS sensor circuit as claimed in  
claim 1, wherein said voltage control circuit  
30 comprises:  
an inverter circuit driving a gate of said  
reset transistor, the inverter circuit including a  
first P-channel MOS transistor and an N-channel MOS  
transistor; and  
35 a transistor inserted between a drain of  
said first P-channel MOS transistor and a drain of  
said N-channel MOS transistor so as to control a

blooming.

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4. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said  
10 reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor inserted between a drain of said first P-channel MOS transistor and a drain of  
15 said N-channel MOS transistor so as to control a blooming.

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5. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said  
25 reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor connected to a drain of said N-channel MOS transistor so as to control a blooming.

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6. The CMOS sensor circuit as claimed in  
35 claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said

reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

5 a transistor connected to a drain of said N-channel MOS transistor so as to control a blooming.

10 7. The CMOS sensor circuit as claimed in claim 3, further comprising a plurality of serially connected transistors inserted between said drain of said first P-channel MOS transistor and said drain of said N-channel MOS transistor so as to control  
15 the blooming.

20 8. The CMOS sensor circuit as claimed in claim 4, further comprising a plurality of serially connected transistors inserted between said drain of said first P-channel MOS transistor and said drain of said N-channel MOS transistor so as to control  
25 the blooming.

30 9. The CMOS sensor circuit as claimed in claim 5, further comprising a plurality of serially connected transistors connected to said drain of said N-channel MOS transistor so as to control the blooming.

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10. The CMOS sensor circuit as claimed in claim 6, further comprising a plurality of serially connected transistors connected to said drain of said N-channel MOS transistor so as to control the  
5 blooming.

10 11. The CMOS sensor circuit as claimed in claim 3, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor.

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12. The CMOS sensor circuit as claimed in claim 4, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS  
20 transistor.

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13. The CMOS sensor circuit as claimed in claim 3, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain  
30 connected to each other.

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14. The CMOS sensor circuit as claimed in claim 4, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS

transistor, and includes a gate and a drain connected to each other.

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15. The CMOS sensor circuit as claimed in claim 5, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

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16. The CMOS sensor circuit as claimed in claim 6, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

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17. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

18. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

5 an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

10 one of a resistance element and a diode element inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

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19. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

20 an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

25 one of a resistance element and a diode element connected to a drain of said N-channel MOS transistor so as to control a blooming.

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20. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

35 an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode

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element connected to a drain of said N-channel MOS transistor so as to control a blooming.

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21. The CMOS sensor circuit as claimed in claim 17, wherein said resistance element and said diode element are replaced by a plurality of  
10 serially connected resistance elements and a plurality of serially connected diode elements, respectively.

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22. The CMOS sensor circuit as claimed in claim 18, wherein said resistance element and said diode element are replaced by a plurality of  
20 serially connected resistance elements and a plurality of serially connected diode elements, respectively.

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23. The CMOS sensor circuit as claimed in claim 19, wherein said resistance element and said diode element are replaced by a plurality of  
30 serially connected resistance elements and a plurality of serially connected diode elements, respectively.

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24. The CMOS sensor circuit as claimed in

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producing said first signal by delaying said second signal.

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28. The CMOS sensor circuit as claimed in claim 26, further comprising a delay circuit producing said first signal by delaying said second signal.

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29. The CMOS sensor circuit as claimed in claim 27, said delay circuit is formed by an even number of inverters.

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30. The CMOS sensor circuit as claimed in claim 28, said delay circuit is formed by an even number of inverters.

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31. The CMOS sensor circuit as claimed in claim 3, an arbitrary bias voltage is applied to said transistor.

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32. The CMOS sensor circuit as claimed in claim 4, an arbitrary bias voltage is applied to

said transistor.

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33. The CMOS sensor circuit as claimed in claim 5, an arbitrary bias voltage is applied to said transistor.

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34. The CMOS sensor circuit as claimed in claim 6, an arbitrary bias voltage is applied to said transistor.

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35. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises an output node connected to a gate of said reset transistor, and a constant current source added to said output node.

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36. The CMOS sensor circuit as claimed in claim 35, wherein said constant current source is formed by a second P-channel MOS transistor having a bias voltage applied to a gate voltage thereof.

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